REMARKS

Applicants appreciate the Examiner's thorough review of the present application, and respectfully request reconsideration in light of the preceding amendments and the following remarks.

Claims 5 and 24-26 are pending in the application.

Claim 5 has been amended to include all limitations of original claim 6. That is, amended claim 5 additionally recites that the first and second conductive GaN clad layers are n-doped and p-doped GaN clad layers, respectively. Claim 5 has further been amended to include the limitation that the first conductive GaN clad layer which is **an n-doped GaN clad layer is in direct contact with the first contact.** This limitation is supported by the specification and the drawing, e.g., at page 10, lines 24-26, and FIG. 2 where it is disclosed that the n-type GaN clad layer 25c is in directed contact with the n-type contact 29.

Claims 18-23 have been cancelled without prejudice or disclaimer. New claims 24-26 corresponding to original claims 2-4 have been added to provide Applicants with the scope of protection to which they are believed entitled.

No new matter has been introduced through the foregoing amendments.

Amended claim 5 is patentable over the applied references for the following reasons.

The primary reference of *Miura* fails to disclose or suggest that the first conductive GaN clad layer (n-doped GaN clad layer) is in direct contact with the first contact. In the *Miura* device, the n-doped GaN layer is layer 3. *See Miura* at FIG. 1 and column 7, lines 22-23. However, there are a buffer layer 2 and a GaAs substrate 1 located between the n-type GaN layer 3 and the first contact 7. Buffer layer 2 and/or substrate 1 greatly deteriorate the ohmic contact property between the n-type GaN layer 3 and the contact 7. In contrary, according to the claimed

invention, since the n-doped GaN clad layer is in direct contact with the first contact, the ohmic contact property is enhanced.

In addition, *Miura* fails to disclose or suggest the conductive substrate of claim 5 which is located between the second conductive GaN clad layer (p-doped GaN clad layer) and the <u>second</u> contact. *See* 25a, 21 and 27 in FIG. 2 of the instant application. In the *Miura* device, the GaAs substrate 1 is disposed between the n-type GaN layer 3 and the <u>first</u> contact 7, and there is no conductive substrate between the p-type GaN layer 5 and the second contact 6. *See* FIG. 1 in *Miura*.

The Examiner admitted that *Miura* does not teach or suggest the claimed conductive adhesive layer of Au-Sn, Sn, In, Au-Ag or Pb-Sn. The Examiner is relying on *Keizo* and *Ishida* for the missing elements. The Examiner's suggested combination is improper for the reasons advanced in the previous amendment papers which are incorporated herein by reference. However, even if the Examiner's suggested combination is proper, the combined references would still lack, at least, the limitation newly added to claim 5.

In particular, *Keizo* does not disclose or suggest a vertical GaN-based light emitting diode. The *Keizo* device is not a GaN-based device; it is a AlGaInP or AlGaAs light emitting device. For this reason alone, *Keizo* is not deemed combinable with *Miura*.

Assuming *arguendo* that the *Miura* device is modifiable to include the adhesive layer 3 or 3' disclosed in *Keizo* at FIGs. 1, 2, 6, 7, 8, 11, 12, the combined device would still fail to teach or disclose all limitations of amended claim 5for the following reasons.

First, if the *Miura* device is modified to include the adhesive layer 3 of *Keizo* (FIG. 1(b), 2, 6, 7 or 8 in *Keizo*), <u>the *Keizo* adhesive layer 3 would be inserted between the *Miura* n-type GaN layer 3 and buffer layer 2 or between the *Miura* buffer layer 2 and substrate 1</u>. In addition, <u>the combined device would fail to include the n-type GaN layer 3 being in direct contact with the</u>

first contact 7, due to the *Miura* buffer layer 2 and substrate 1 located between the n-type GaN layer 3 and the contact 7.

The claimed invention, as exemplified by the embodiment shown in FIG. 2 of the instant application, however, includes a conductive adhesive layer (e.g., 22 or 24) located between the second conductive GaN clad layer (e.g., p-doped GaN clad layer 25a) and the substrate (e.g., 21), with the n-doped GaN clad layer (e.g., 25c) being in direct contact with the first contact (e.g., 29) resulting in a superior ohmic contact property.

Second, if the *Miura* device is modified to include the adhesive layer 3' of *Keizo* (FIGs. 1(a), 11 or 12 in *Keizo*), the *Miura* n-type GaN layer 3 cannot be in direct contact with the first contact 7, due to the buffer layer 2. Applicants note that the GaAs substrate 61 of *Keizo* is removed by 'wet etching' in order to form the n-contact 5 (corresponding to the claimed first contact) on the n^+-AlGaAs layer 44', after attaching the conductive substrate 2 to the light emitting structure 4' by using the adhesive layer 3'. *See Keizo* at FIGs. 3(c), 3(d) 11, and paragraphs [0030], [0031]. Such a wet etching process cannot remove GaN material such as the buffer layer 2 of *Miura*. Therefore, the *Miura* buffer layer 2 remains between the n-type GaN layer 3 and the first contact 7 when *Miura* is modified with the *Keizo* adhesive 3', resulting in a degradation in ohmic contact.

In addition, the Examiner's suggested combination of *Miura* and *Akita* also fails to teach or disclose the light emitting diode of amended claim 5. The reason is that even if the *Miura* device is modifiable to include the adhesive layer 7 of *Akita* (FIG. 1 in *Akita*), the *Miura* n-type GaN layer 3 cannot be in direct contact with the first contact 7, due to the buffer layer 2. Since the GaAs, InP, InAs or GaP substrate of *Akita* is removed by 'wet etching', the *Miura* GaN buffer layer 2 remains as discussed above with *Miura* and *Keizo*. *See* FIG. 1, and paragraphs [0013] and [0014] of *Akita*. Therefore, the *Miura* buffer layer 2 remains between the n-type GaN

layer 3 and the first contact 7 when *Miura* is combined with *Akita*, resulting in a degradation in ohmic contact.

Similarly, the proposed combination of *Miura*, *Keizo* and *Akita* does not teach or disclose the diode of amended claim 5 having the n-GaN clad layer in direct contact with the first contact.

Accordingly, Applicants respectfully submit amended claim 5 is patentable over the applied references. Claims 24-26 depend from claim 5, and are considered patentable at least for the reason advanced with respect to amended claim 5.

Each of the Examiner's rejections has been traversed/overcome. Accordingly, Applicants respectfully submit that all claims are now in condition for allowance. Early and favorable indication of allowance is courteously solicited.

The Examiner is invited to telephone the undersigned, Applicant's attorney of record, to facilitate advancement of the present application.

Application No.: 10/601,597 **Docket No.: 2336-181**

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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571-273-8300
FACSIMILE NUMBER